Reliability of gate oxides in 3D-architectures (FinFETs, Nanowires)

X. Garros[1], A. Laurent[1], S. Barraud[1], M. Casse[1], F. Gaillard

[1] *CEA-LETI, Grenoble Alpes University, Grenoble, France*

xavier.garros@cea.fr

Abstract

The impact of 3D architectures and boosters on the reliability is deeply investigated in this paper. BTI geometry is first studied and is shown to be dependent of the quality of the sidewalls interface. Moreover it is found that "Ωfet" also offers a better overall BTI reliability than Πfet. Finally strained SOI & SiGeOI devices are highly suitable since they allow boosting the transistor performance without any reliability penalty.

1. Introduction

3D technologies are a major breakthrough in semiconductor industry [1,2]. If it is obvious that 3D transistors offer enhanced performance, it is unclear whether the 3D architecture (square or circle shape, aspect ratio,…) is the best suitable to maintain a high level of reliability. In this paper, we investigate how device architecture and mobility boosters impact both the performance & reliability of 3D devices. Firstly Bias Temperature Instability (BTI) and Hot Carrier (HC) reliability are deeply investigated in N&PMOS with several shapes and geometries. Then the impact of mobility boosters as Strained Si & SiGe is addressed.

2. Experimental

HK/MG silicon Nanowires (NW) are fabricated on FDSOI substrates using the process described in [3]. The dielectric stack consists of a thin SiO_2/HfSiON gate oxide and of a TiN metal gate. The buried oxide is 145nm thick. This standard process flow leads to a square shaped NW transistor called here "Πfet" (Fig.1a). The top surface width and the height of the NW are denoted W_{top} and t_{Si} respectively. For the standard Πfet, t_{Si} is ~12nm and the crystalline orientations of the sidewalls SW and the top surface TS are <110> & <100> respectively. The effective width W_{eff} is defined here as its perimeter $\sim 2t_{Si}+W_{top}$. By increasing t_{Si}, it is possible to switch from a "Πfet" device with $t_{Si}/W_{top}\sim 1$ to a "Finfet" structure (Fig.1b) with much higher aspect ratio >2. On the other hand increasing W_{top} up to >100nm turns the NW Πfet into a planar FDSOI device (Fig.1c). Tested structures are either single or multiple parallel transistors. BTI&HCI measures are performed at T=125°C on 10dies per condition.

3. Results and Discussion

The impact of scaling on BTI is first analyzed (Fig.2). PBTI is almost independent of device width W_{top} and t_{Si}. Unlike PBTI, NBTI strongly increases with W_{top} scaling (Fig.3). The NBTI enhancement is spectacular since it is more than 100% between large and narrow devices (Fig.4) and is observed on both Πfet and Finfet. Several reasons were proposed to explain this effect also reported in Finfet technology [4-10]. The first one is as a possible increase of the oxide field in the device corners [6-8]. TCAD simulations of Fig.5 show that no enhanced field is noticeable in the corners of both planar and NW devices. This rules out this hypothesis to explain the NBTI geometry dependence. Fig.6 rather suggests that the NBTI enhancement is actually due to a poorer quality of the SW compared to the TS [9]. Indeed the "surface roughness limited" mobility measured at low temperature is clearly degraded in narrow transistors w.r.t. wide devices [10]. This poorer quality is not related to SW orientations but rather results from a higher surface roughness of the SW induced by the device processing (oxide deposition, etching). This last point is further confirmed by means of electrostatic simulations of NBTI trapping in 3D structures illustrated in Fig.7&8. By analyzing how a single punctual charge q impacts the V_T of 3D devices, we notice a strong difference between NW Πfet, Finfet and planar device that leads to various contributions of SW & TS on individual ΔV_T. Fig.9 confirms that a higher SW density (x2.5) compared to TS is a reasonable explanation for enhanced NBTI in narrower devices. Fig.10 summarizes our findings about BTI. Then we analyze how the shape of the transistor affects its reliability. H_2 annealing is performed to turn a Πfet device into a Ωfet with almost circular section (Fig.11). Short channel performance are identical (Fig.12). Regarding reliability, NBTI is slightly improved in Ωfet whereas PBTI is degraded (Fig.13). However, as NBTI degradation is much higher than PBTI at same overdrive, Ωfet transistors exhibit an overall better BTI reliability. Finally the impact of mobility boosters on performance and reliability is investigated. To do that, we fabricate NMOS strained SOI (sSOI) and PMOS SiGeOI nanowires (Fig.14). As expected, performance is boosted in sSOI or SiGeOI (Fig.15). BTI reliability is also clearly better for both sSOI and SiGeOI devices at same overdrive (Fig.16). For NMOS, this may result from the reduction of leakage current by strain [11] and a favorable alignment of the SiGe Fermi level w.r.t. the oxide defect energy levels [12]. For HC reliability, sSOI and SiGeOI offer a much better performance/reliability compromise visible in Fig.17.

4. Conclusion

We deeply investigate the impact of several 3D architectures (Πfet, Finfet, Ωfet) as well as mobility boosters on transistor performance & reliability. (1) PBTI is independent of the geometry whereas NBTI is strongly enhanced in narrow devices (2) Ωfet is also beneficial w.r.t. Πfet due to BTI reduction (3) Mobility boosters like sSOI & SiGe are highly suitable since their integration does not induce reliability penalty.

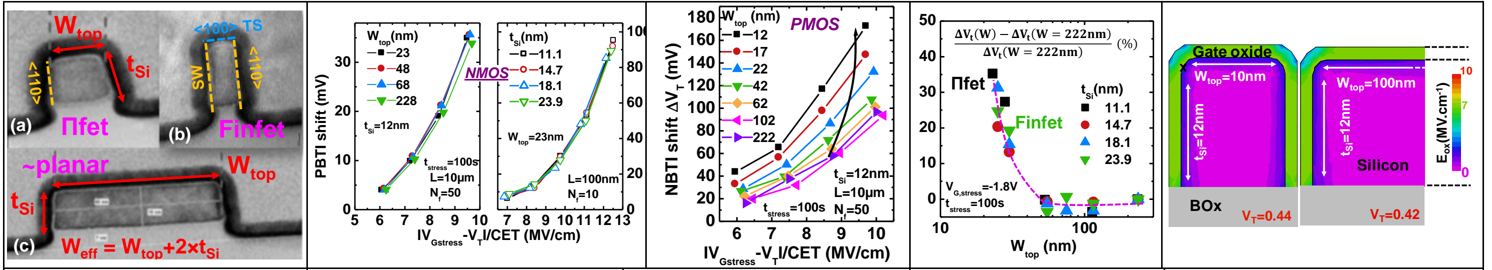

Fig. 1. Cross sectional TEM images of a standard square shaped "Πfet", "Finfet" or wide planar FDSOI transistor"

Fig. 2. PBTI shift vs oxide field for various (left) top widths (right) silicon thicknesses. PBTI is almost independent of the NMOS device geometry.

Fig. 3. NBTI shift vs oxide field for various W_{top}. Unlike PBTI, NBTI is strongly enhanced in narrow PMOS transistors

Fig. 4. NBTI variation vs W_{top} for various t_{Si}. Degradation is slightly higher in Finfet (t_{Si}>20nm) than in Πfet (t_{Si}=11nm)

Fig. 5. 3D electrostatic simulation of oxide field in a (left) narrow and (right) wide device @V_G=1.6V. No enhanced E_{ox} in the corners is visible

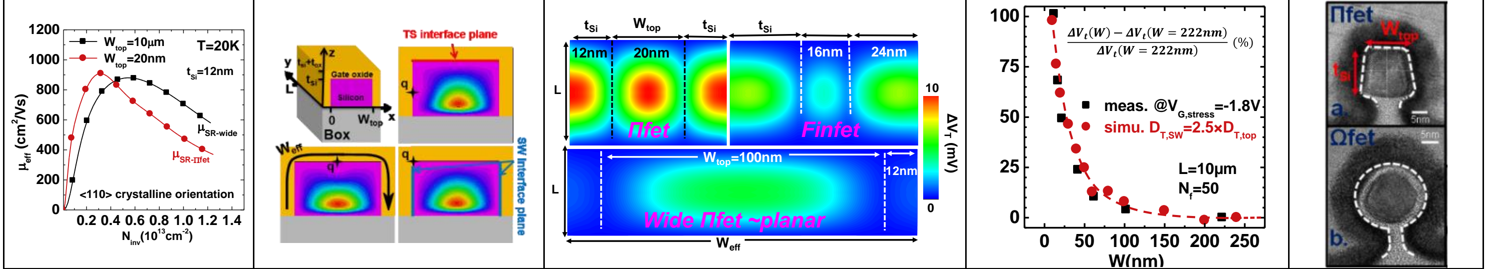

Fig. 6. Surface roughness limited mobility μ_{SR} for narrow and wide devices. Lower mobility in 20nm Πfet supports the idea of a degradation of the SW interface due to process

Fig. 7. Cross sectional carrier densities in a Πfet at y=L/2. The variation of the carrier density induced by q depends on its position along SW & TS interface planes.

Fig. 8. Top view of the individual ΔV_t (see Fig.13) for Πfet, Finfet and Planar FDSOI devices. The ratio of the magnitude of SW and TS peaks depends on device geometry. For wide transistor, the effect of SW becomes negligible

Fig. 9. Measured and simulation of the NBTI enhancement. A perfect agreement is found when D_t^{SW} is fixed 2.5 higher than D_t^{TS}

Fig. 11 Cross sectional TEM images of a (a) square shaped "Πfet" (b) "Ωfet" after H_2anneal

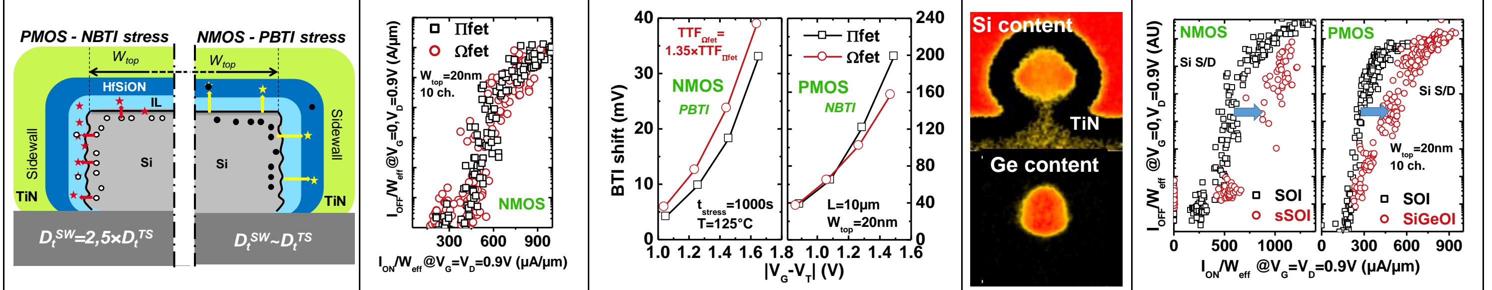

Fig. 10. Physical mechanisms responsible for BTI geometry dependence. NBTI variation with W_{top} results from a x2.5 higher IL trap density on the SW due to fabrication process. PBTI is not affected because e- trapping occurs in the HK layer

Fig. 12 (I_{ON}-I_{OFF})/W_{eff} for short channel (left) SOI & sSOI (right) SOI & SiGeOI Πfet devices.

Fig. 13. Effect of "rounding" on both PBTI & NBTI. Unlike PBTI, NBTI is improved for Ωfet at high stress biases

Fig. 14. EDX analysis of a SiGeOI device

Fig. 15. (I_{ON}-I_{OFF})/W_{eff} for short channel (left) SOI & sSOI (right) SOI & SiGeOI Πfet devices.

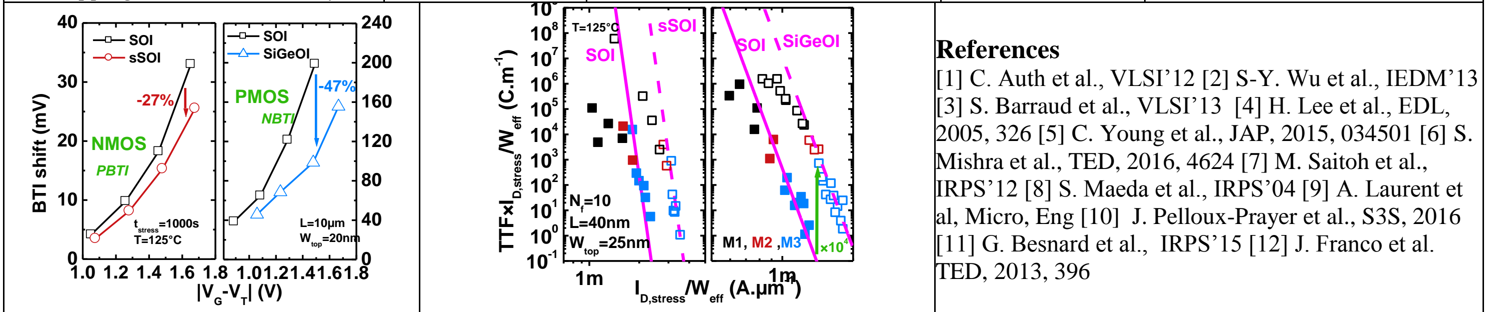

Fig. 16. BTI reliability (left) SOI vs sSOI n-NWs (right) SOI vs SiGeOI p-NWs. Both mobility boosters improve BTI reliability

Fig. 17 HC reliability (left) SOI vs sSOI n-NWs (right) SOI vs SiGeOI p-NWs. Better trade-off Performance/HC reliability in "boost" sSi and SiGe devices

References

[1] C. Auth et al., VLSI'12 [2] S-Y. Wu et al., IEDM'13 [3] S. Barraud et al., VLSI'13 [4] H. Lee et al., EDL, 2005, 326 [5] C. Young et al., JAP, 2015, 034501 [6] S. Mishra et al., TED, 2016, 4624 [7] M. Saitoh et al., IRPS'12 [8] S. Maeda et al., IRPS'04 [9] A. Laurent et al, Micro, Eng [10] J. Pelloux-Prayer et al., S3S, 2016 [11] G. Besnard et al., IRPS'15 [12] J. Franco et al. TED, 2013, 396

Acknowledgments

This work is partly funded by the French Public Authorities through NANO2022 program